Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A method of processing data comprising the step of:

coupling:

(a) at least one unit adapted for processing data in a sequential manner and comprising an instruction pipeline; and

(b) an array adapted for processing data, the array comprising a plurality of data processing cells having programmable coarse grained arithmetic logic units (ALUs) ~~that are configurable in their function~~ and the array comprising a packet-oricnted ~~configurable~~ nctwork communicating values in packets;

wherein:

the at least one unit is operable independently of the array; and

the array:

processes at least one program that is compiled from a high-level language; and

is:

at least one of coarse grained and runtime reconfigurable; and

controlled by instructions issued from ~~coupled to~~ the instruction pipeline of the at least one unit to the array.

2. (Currently Amended) A method according to claim 1, further comprising the step of:

transferring via at least one data path at lcast one of an input data and an output data from the at least one unit to the array and from the array to the at least one unit, the at least one data path being provided therebetween and comprising at least one FIFO so as to allow for at least one of (i) a coupling between the at least one unit and the array that is not ~~strictly~~ synchronous and (ii) a data processing within the at least one unit and the array that is not ~~strictly~~ synchronous.

3. (Previously Presented) A method according to claim 2, wherein the transferring is performed by at least one of inserting data directly into and extracting data directly from a data path of at least one of the at least one unit and the array.

4. (Previously Presented) A method according to claim 3, further comprising the step of:

providing between the at least one unit and the array a path adapted for transfer of at least one of status information and event information.

5. (Previously Presented) A device for processing data comprising:

at least one unit adapted for processing data in a sequential manner and comprising an instruction pipeline; and

an array adapted for processing data comprising a configurable network and a plurality of data processing cells that are configurable in their function;

wherein:

the array is coupled to the instruction pipeline, the coupling of the array to the instruction pipeline including controlling configurations by the instruction pipeline; and

the at least one unit is operable independently of the array.

6. (Currently Amended) The device according to claim 5, wherein at least one of:

at least one data path is provided between the array and the at least one unit, the at least one data path comprising at least one FIFO that allows at least one of (i) a coupling between the at least one unit and the array that is not ~~strictly~~ synchronous and (ii) a data processing within the at least one unit and the array that is not ~~strictly~~ synchronous; and

data is transferred by at least one of extracting data directly from and inserting data directly into a data path of at least one of the at least one unit and the array.

7. (Previously Presented) A method of processing data comprising the steps of: coupling:

(a) at least one unit adapted for processing data in a sequential manner and comprising an instruction pipeline; and

(b) an array that:

is adapted for processing data; ~~, the array comprising~~

comprises a plurality of data processing cells having programmable coarse grained arithmetic logic units (ALUs); ~~that are configurable in their function and the array comprising~~

comprises a packet-oriented ~~configurable~~ network communicating values in packets; and

processes at least one program that is compiled from a high-level language; and

providing a path allowing for block data transfer between ~~from~~ the array and the at least one unit through [[of]] a data cache ~~and another data source~~.

8-11. (Canceled).

12. (Previously Presented) A method according to claim 1, wherein the at least one unit includes at least one of a CPU, a von-Neumann-Processor, and a microcontroller.

13. (Previously Presented) A method according to claim 1, wherein the array includes at least one of a data processor, a Field Programmable Gate-Array (FPGA), a Data Flow Processor (DFP), a Digital Signal Processor (DSP), an eXtreme Processing Platform (XPP), and a chaemeleon-technology data processing fabric.

14. (Previously Presented) A method according to claim 2, wherein the at least one data path between the at least one unit and the array includes at least one local memory connected to the at least one unit as a cache and connected to the array.

15. (Previously Presented) A method according to claim 14, wherein the at least one local memory includes an internal RAM (IRAM).

16. (Previously Presented) A method according to claim 1, wherein configuration information for the array is issued by the instruction pipeline of the at least one unit.

17. (Currently Amended) A method according to claim 16, further comprising:

buffering the configuration information in at least one FIFO so as to allow for at least one of a coupling between and a data processing within the at least one unit and the array that is not ~~strictly~~ synchronous.

18. (Previously Presented) A method according to claim 1, wherein the at least one unit supports multi-threading, and the array is connected as a thread unit.

19. (Previously Presented) A method according to claim 18, wherein the array is operable synchronously to the unit.

20. (Previously Presented) A method according to claim 4, wherein the at least one of the status information and the event information includes at least one of flags, an overflow, and a carry.

21. (Previously Presented) A device according to claim 5, wherein the at least one unit includes at least one of a CPU, a von-Neumann-Processor, and a microcontroller.

22. (Previously Presented) A device according to claim 5, wherein the array includes a runtime reconfigurable data processor.

23. (Previously Presented) A device according to claim 6, wherein the at least one data path includes at least one local memory connected to the unit as cache and connected to the array.

24. (Previously Presented) A method according to claim 23, wherein the at least one local memory includes an internal RAM (IRAM).

25. (Previously Presented) A device according to claim 5, wherein configuration information for the array is issued by the instruction pipeline.

26. (Currently Amended) A device according to claim 25, wherein the configuration information is buffered in at least one FIFO so as to allow for at least one of (i) a coupling between the at least one unit and the array that is not ~~strictly~~ synchronous and (ii) a data processing within the at least one unit and the array that is not ~~strictly~~ synchronous.

27. (Previously Presented) A device according to claim 5, wherein the at least one unit supports multi-threading, and the array is connected as a thread unit.

28. (Previously Presented) A device according to claim 27, wherein the array operates synchronously to the unit.

29. (Previously Presented) A method according to claim 7, wherein the at least one unit includes at least one of a CPU, a von-Neumann-processor, and a microcontroller.

30. (Previously Presented) A method according to claim 7, wherein the array includes at least one of a runtime and reconfigurable data processor, a Data Flow Processor (DFP), a Digital Signal Processor (DSP), an eXtreme Processing Platform (XPP), and a chaemeleon-technology data processing fabric.

31. (New) A method according to claim 7, wherein the array is controlled by instructions issued from the instruction pipeline of the at least one unit to the array.

32. (New) A method according to claim 7, wherein the array is controlled by instructions issued from the instruction pipeline of the at least one unit directly to the array.

33. (New) A method according to claim 7, wherein a packet oriented data bus in the array is configurable.

34. (New) A method according to claim 33, wherein the packet oriented data bus in the array is reconfigurable.

35. (New) A method according to claim 33, wherein the packet oriented data bus in the array is reconfigurable at runtime.

36. (New) A method according to claim 7, wherein the cells are configurable.

37. (New) A method according to claim 7, wherein the packet oriented network is configurable.

38. (New) A method according to claim 7, wherein the cells are runtime reconfigurable.

39. (New) A method according to claim 7, wherein the packet oriented network is runtime reconfigurable.

40. (New) A method according to claim 1, wherein the instructions are issued from the instruction pipeline of the at least one unit directly to the array.

41. (New) A method according to claim 1, wherein the at least one unit and the array exchange data via a joint D-cache.

42. (New) A method according to claim 1, wherein the at least one unit transmits data directly from within the data path to the array.

43. (New) A method according to claim 1, wherein the at least one unit transmits data directly from a Write stage of the data path to the array.

44. (New) A method according to claim 1, wherein the array transmits data directly into the data path of the at least one unit.

45. (New) A method according to claim 1, wherein the array transmits data directly into an Execute stage of the data path of the at least one unit.

46. (New) A method according to claim 1, wherein the array is accessible as a register file in the at least one unit.

47. (New) A method according to claim 1, wherein the array is accessible in parallel to the register file in the at least one unit.

48. (New) A method according to claim 1, wherein data is transferred between the at least on unit and the array via FIFOs.

49. (New) A method according to claim 1, wherein data is transferred between the at least on unit and the array via dual-clock FIFOs.

50. (New) A method according to claim 1, wherein a packet oriented data bus in the array is configurable.

51. (New) A method according to claim 50, wherein the packet oriented data bus in the array is reconfigurable.

52. (New) A method according to claim 50, wherein the packet oriented data bus in the array is reconfigurable at runtime.

53. (New) A method according to claim 1, wherein the cells are configurable.

54. (New) A method according to claim 1, wherein the packet oriented network is configurable.

55. (New) A method according to claim 1, wherein the cells are runtime reconfigurable.

56. (New) A method according to claim 1, wherein the packet oriented network is runtime reconfigurable.

57. (New) A method of processing data comprising:

coupling:

(a) at least one unit adapted for processing data in a sequential manner and comprising an instruction pipeline; and

(b) an array that:

is adapted for processing data;

comprises a plurality of data processing cells having programmable coarse grained arithmetic logic units (ALUs);

comprises a packet oriented network communicating values in packets; and

processes at least one program that is compiled from a high-level language;

wherein the at least one unit is operable independently of the array and transmits data directly from within a data path of the at least one unit to the array.

58. (New) A method according to claim 57, wherein the array is controlled by instructions issued from the instruction pipeline of the at least one unit to the array.

59. (New) A method according to claim 57, wherein the array is controlled by instructions issued from the instruction pipeline of the at least one unit directly to the array.

60. (New) A method according to claim 57, wherein the at least one unit transmits data directly from a Write stage of the data path to the array.

61. (New) A method according to claim 57, wherein the array transmits data directly into the data path of the at least one unit.

62. (New) A method according to claim 57, wherein the array transmits data directly into an Execute stage of the data path of the at least one unit.

63. (New) A method according to claim 57, wherein the array is accessible as a register file in the at least one unit.

64. (New) A method according to claim 57, wherein data is transferred between the at least on unit and the array via FIFOs.

65. (New) A method according to claim 57, wherein data is transferred between the at least on unit and the array via dual-clock FIFOs.

66. (New) A method according to claim 57, wherein the array is accessible in parallel to a register file in the at least one unit.

67. (New) A method according to claim 57, wherein a packet oriented data bus in the array is reconfigurable.

68. (New) A method according to claim 57, wherein a packet oriented data bus in the array is reconfigurable at runtime.

69. (New) A method according to claim 57, wherein the cells are configurable.

70. (New) A method according to claim 57, wherein the packet oriented network is configurable.

71. (New) A method according to claim 57, wherein the cells are runtime reconfigurable.

72. (New) A method according to claim 57, wherein the packet oriented network is runtime reconfigurable.